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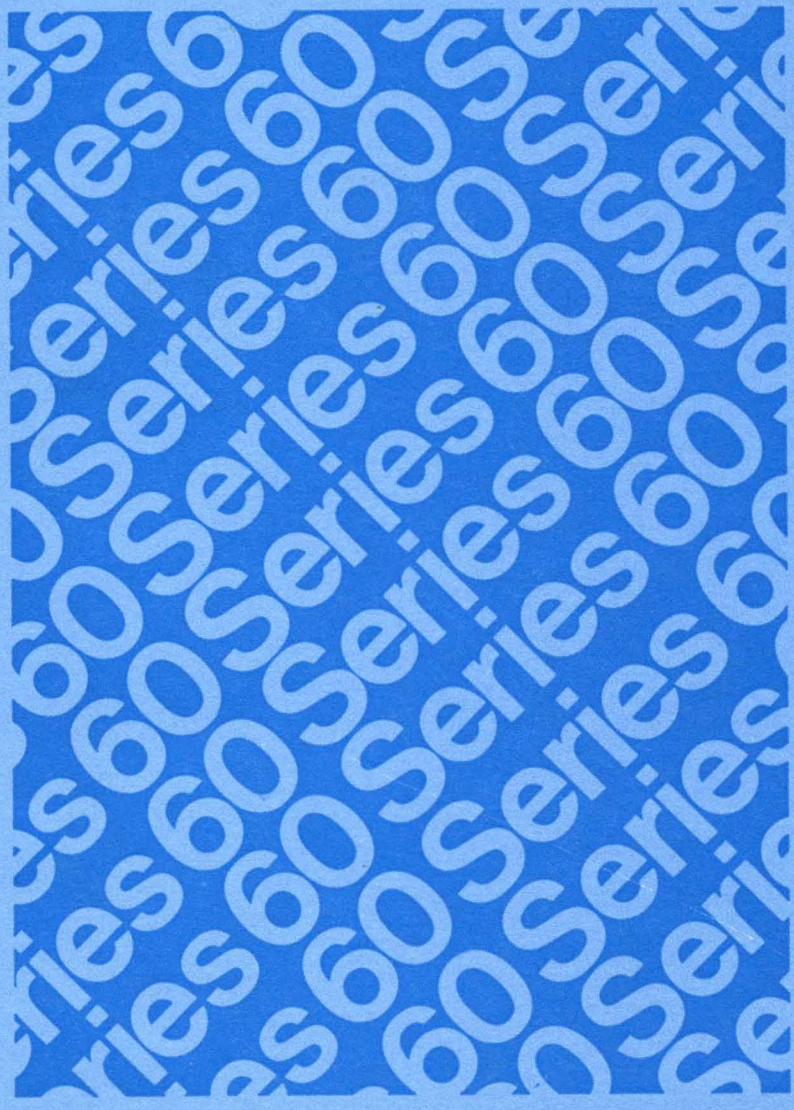

LEVEL 6

HARDWARE

MSU9101/9102/ 9103/9104/9105/ 9106 MASS STORAGE SUBSYSTEM OPERATION

SERIES 60 (LEVEL 6)

MSU9101/9102/9103/9104/9105/9106 MASS STORAGE SUBSYSTEM OPERATION

SUBJECT

General Description, Programming, Operation and Maintainance Procedures for the MSU9101/9102/9103/9104/9105/9106 Mass Storage Units

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Preface

This reference document provides hardware-oriented descriptive and instructive material for the user of the MSU9101/9102/9103/9104/9105/9106 Mass Storage Units and others concerned with their technical aspects, application, or use.

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Section 1
General Description

The MSU9101/9102/9103/9104/9105/9106 Mass Storage Units are high-capacity, high-performance removable disk units for Level 6 Model 33 and larger systems (see Figure 1-1). The MSU9101 and MSU9102 units have formatted (long/short sectors) storage capacities of 37/33MB and 75/67MB, respectively. Both units include a free-standing cabinet with room for one additional unit of either 37/33MB (MSU9105) or 75/67MB (MSU9106). The MSU9103 and MSU9104 units have formatted storage capacities of 144/128MB and 288/256MB, respectively. Both units include a free-standing cabinet capable of housing a single unit. Subsystem storage capacity ranges from 33MB to 1152MB for a maximum of four units.

Information can be recorded in either 411 or 823 cylinders of data on 5 or 19 recording surfaces. Under software control, each track can be formatted into either 8 sectors of 2304 bytes or 64 sectors of 256 bytes. The latter, which is the format utilized by standard Honeywell software, results in smaller quoted capacities for each model (see Table 1-1).

The units interface to the Level 6 Megabus via a single-board Mass Storage Controller (MSC9102) and a device adapter. Each unit includes a 30-foot cable that attaches to the single common device adapter connected to the MSC, which in turn plugs into a slot on the Level 6 Megabus. Additional cables (as noted in Table 1-1) are also provided.

MSU9101/9102/9105/9106 MSU9103/9104

Figure 1-1. Mass Storage Units

DATA INTEGRITY AND PROTECTION

The integrity and protection of data is ensured by the following features:

- *Write protect capability* — Individual write protect button for each disk unit eliminates the possibility of recording on protected files.
- *Automatic unloading* — Heads automatically unload when specific conditions, such as low rotational speed or loss of power, are detected.
- *Power fault sensing* — If an ac or dc power fault has occurred, recording cannot take place.
- *Write current monitoring* — Write current is inhibited during seeks or without a command, and loss is detected during a write command.
- *EDAC recording* — The validity of recorded information is ensured by the system which uses Error Detection and Correction recording.
- *Head and read strobe* — Head and read strobe may be offset by command to facilitate data recovery.
- *No/multihead select* — The device checks for no/multi heads being selected, which would inhibit the write function.

SYSTEM AVAILABILITY

Disk unit, device-pac, or controller malfunctions are easily and quickly isolated to their Optimum Replaceable Unit (ORU). Boards within the central subsystem that have microprogramming (firmware) like the MSC9102, have built-in self-checking capabilities called QLTs (Quality Logic Tests) and LEDs (Light-Emitting Diodes) for problem indication. The QLTs are initiated in the MSC and elsewhere in response to a Master Clear or an Initialize command. The LEDs on the associated boards are lit, and after internal checking is finished, the lights are extinguished one after another. Any LED remaining lit indicates a malfunction on that board and the CHECK light on the operator's panel is lit to inform the operator.

More comprehensive testing is available to the operator via the test and verification (T&V) programs. The T&Vs are loaded and run when it is necessary to verify all operational aspects of the

MSC and isolate failures to the MSC, device adapter, or disk unit. Reference the *Level 6 Model 3X, 4X, 5X System Checkout T&V Operator's Guide*, Order No. AW94.

SPECIFICATIONS

Table 1-1 lists the specifications for the mass storage units.

TABLE 1-1. MASS STORAGE UNIT SPECIFICATIONS

	MSU9101/ 9105	MSU9102/ 9106	MSU9103	MSU9104
Data Capacity:				
Cylinders/Unit	411	823	411	823
Tracks/Cylinder	5	5	19	19
Sectors/Track	8 or 64	8 or 64	8 or 64	8 or 64
Bytes/Sector	2304 or 256	2304 or 256	2304 or 256	2304 or 256
Capacity/Unit				
2304 bytes/sector	37,877,760	75,847,680	143,935,488	288,221,184
256 bytes/sector	33,669,120	67,420,160	127,942,656	256,196,608
Avg. Latency Time	8.33	8.33	8.33	8.33
Seek Time (ms):				
Minimum (1 cylinder)	6	6	6	6
Average	25	30	25	30
Maximum	45	55	45	55
Transfer Rate:				
Bytes/second	1.2M	1.2M	1.2M	1.2M
Words/second	600K	600K	600K	600K
Disk Pack:	M4130 (ordered separately)		M4190 (ordered separately)	
Number of platters	5 (2 covers; 3 recorded)		12 (2 covers; 10 recorded)	
Number of surfaces	6 (1 servo; 5 data)		20 (1 servo; 19 data)	
Diameter	14.025 in. (35.623 cm)		14.025 in. (35.623 cm)	
Height	4.00 in. (10.16 cm)		7.06 in. (17.93 cm)	
Weight	6.31 lb (2.87 kg)		less than 21 lb (9.53 kg) without cover	
Recording mode	MFM		MFM	
Bit density (inside track)	6038 bpi		6038 bpi	
Track density	384 tpi		384 tpi	
Spindle speed	3600 rpm ± 3.5%		3600 rpm ± 3.5%	

Simultaneity:

During a data transfer on one unit, a simultaneous seek operation can be performed on all other units.

Controller:

Primary board with two secondary boards, requires Megabus slot; requires 14.8 A +5 V, 0.5 A ± 12 V

Cables (supplied with devices):

Radial/controller — 30 ft (to each pair of units)

Daisy chain — controller to first unit, 30 ft; unit to unit, same cabinet (MSU9101/9102/9105/9106), 3 ft; unit to unit, different cabinets, 10 ft

Electrical Characteristics:

Line voltage (MSU9101/9102/9105/9106) — 120 +12, −18 Vac, single phase

Line voltage (MSU9103/9104) — 208 + 14.6, −29 Vac; 230 + 16.0, −32 Vac, single phase

Frequency — 60 ±0.5 Hz

Power consumption per unit (MSU9101/9102/9105/9106) — start (6 s), 3.36 kVA; run, 0.984 kVA

Power consumption per unit (MSU9103/9104) — start (6 s), 7.90 kVA; run, 1.66 kVA

Line cord — 12.0 ft (365.8 cm)

Connector (MSU9103/9104) — 208/230 V, 20 A, 1-phase, 2-pole, 3-wire male connector

UL approved

TABLE 1-1 (CONT). MASS STORAGE UNIT SPECIFICATIONS

Physical Characteristics:

Height — 36.2 in. (92.0 cm)
Depth — 36.0 in. (91.4 cm)
Width — 23.0 in. (58.4 cm)
Weight (MSU9101/ 9102/9105/9106) — 340 lb (154.5 kg) for 1 unit; 517 lb (235.0 kg) for 2 units
Weight (MSU9103/9104) — 500 lb (252 kg)

Environmental Characteristics:

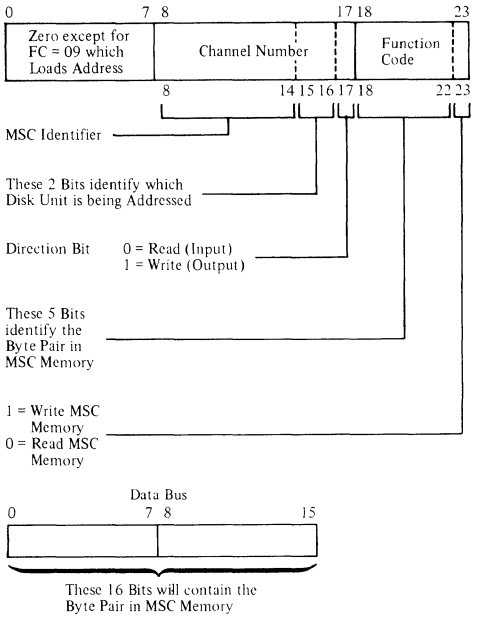
Operating temperature — 50° to 100°F (10°C to 38°C)
Operating relative humidity — 10% to 90% (noncondensing)
Operating temperature gradient — 12°F/hr (6.7°C/hr)

Section 2
Programming

MSC MEMORY AND COMMAND INTERPRETATION

The MSC9102 has a 128-word Read/Write memory that is divided into 32 registers (16 bits per register) for each of the four MSC channels (or ports). The address of each of the various registers in the MSC is a combination of two bits of the channel number and the five high-order bits of the function code used to write into or read from a particular register.

The CP can read or write any register as long as the specific channel is not busy. To write into a register, an I/O *output* command is used; reading is done with an I/O *input* command. Addressing of the various registers relates to the I/O command as follows:



The format shown is for a Write cycle on the bus. For a Read cycle, the memory data will be returned from the MSC on a second bus transfer.

To perform a specific operation, software first loads the address, range, and configuration registers. The task register is loaded last and specifies the operation to be performed. The MSC begins command execution when it receives the task word.

CHANNEL NUMBER

Units attached to the MSC9102 are software addressable via channel numbers. Each disk unit has two such channel numbers assigned, differing only in their low-order bit position called the direction bit.

The channel number for the MSC is separated into three fields:

- MSC Identifier (bits 8-14) — switch selectable and assigned at system installation time.
- MSC Port (bits 15-16) — identifies which of the four disk units is being addressed. Port assignment to a particular disk unit is made when the operator inserts an interchangeable Unit Select Plug into it.
- Direction Bit (bit 17) — specifies in the IOLD command whether it is an input or output data transfer. For all other commands, the direction bit is ignored by the hardware.

SIMULTANEITY

The MSC9102 provides a single level of simultaneity (only one data transfer can be active in the subsystem). However, the MSC will accept a data transfer command to unit B while unit A is performing a data transfer, but will not start the data transfer on B until A's data transfer is completed. Following completion of a data transfer operation, any seek orders received should be initiated prior to the initiation of any data transfer operations. Channels are serviced on a rotating priority basis so that no one channel or channels can dominate MSC usage.

INTERRUPTS

An interrupt will be attemptd whenever a channel interrupt level is not zero, and an operation initiated by an Output Task Word or Output Control Word instruction is completed or the Attention bit is set in the Status Word. If a negative response is received during an interrupt cycle, the MSC will store the interrupt until it can be retried. In the meantime, the MSC can receive commands and/or conduct data transfers on any of the other channels. The channel with the pending interrupt will remain busy and the MSC will not accept any commands issued to that channel except an Output Control Word.

If the interrupt level of a channel is zero (either via initialization or loaded to zero) no interrupts will be attempted for that channel. If a condition or event occurs that would normally cause an interrupt, the appropriate bits in the Status Words will

be set, but no interrupt will be attempted or accepted.

If the interrupt level is set to zero when an interrupt is pending via an Output Control Word (Initialize) or a Master Clear, the pending interrupt will be discarded.

DATA FORMAT

Each track on the disk contains 64 or 8 equal length sectors of 256 or 2304 bytes, respectively. There are 411 or 823 cylinders per surface and 5 or 19 tracks (not including a servo track) per cylinder. The total formatted device capacity varies from 33,669,120 to 1,152,884,736 bytes, dependent on the unit and format.

The data encoding scheme is Modified Frequency Modulation (MFM) recording. Each sector is preceded by an Address Mark, and each field is preceded by a sync word. The sector ID field is followed by error detection bytes and the data field is followed by Error Detection and Correction (EDAC) bytes. The sector ID fields are software programmable and do not have to be numerically sequential with the following exceptions:

1. If the automatic seek function is used, the first three bytes of the ID field must be physical.
2. If the Rotational Position Sensing (RPS) function is used, the fourth byte of the ID field must be physical.

Note that the fourth byte of the sector ID fields will be treated by the MSC as a sector number (see Figure 2-1).

When a track is formatted, 64 or 8 sectors are written beginning at the sector following the Index Mark. The sector IDs are specified by software and are extracted from memory during the format operation. Data fields will be zero filled during formatting.

TRACK FORMAT

The disk track format is shown in Figure 2-1.

Gap 0

The field begins at the trailing edge of the Index-Mark, and consists of 16 bytes of zeros.

Gap 1

The field begins a sector and is made up of 30 bytes as follows:

- 16 bytes of zeros followed by,
- 3 bytes of Address Mark (AM) followed by,
- 10 bytes of zeros followed by,
- 1 sync byte consisting of the hex character 19

Sector Identifier

This is a four-byte field which is formatted as shown in Figure 2-1. The cylinder number is a 10-bit binary number (right justified in bytes 1 and 2) which represents the logical cylinder number from 000, for the outermost track, to 410 or 822 for the innermost track. The track number is a five-bit binary number (right justified in byte 3) which represents one of five or 19 possible data surfaces. The sector number is a binary number (right justified in byte 4) which represents the sector address.

Error Detection Code (EDC)

The two EDC bytes are hardware generated. ID bytes and sync bytes are used during EDC generation and verification. The EDC algorithm used is a half-add.

Gap 2

The field begins following the last byte of the ID EDC bytes and is made up of 14 bytes as follows:

- 13 bytes of zeros (including a one byte end of field pad) followed by,
- 1 sync byte consisting of the hex character 19

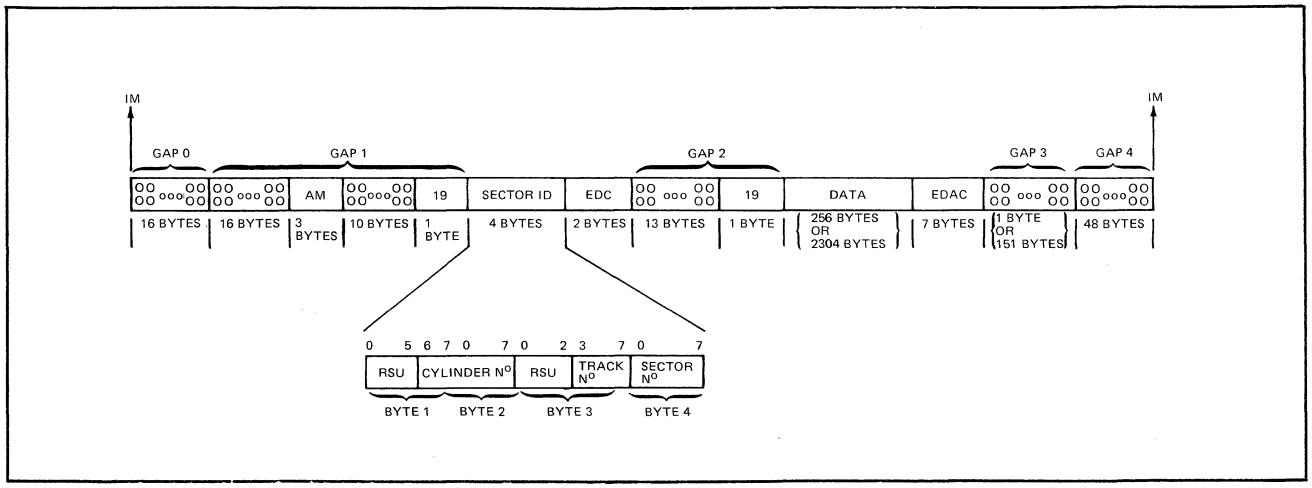


Figure 2-1. Track Format

Data Field

Data fields are either 256 or 2304 bytes long. Any write operation that does not write a complete data field will result in the remainder of the field being zero filled. The Format Write command causes all the data fields on a particular track to be zero filled.

Error Detection and Correction Code (EDAC)

The seven EDAC bytes are hardware generated. Data bytes and sync bytes exclusively are used during EDAC generation and verification. EDAC provides for the correction of error bursts of up to 11 bits and detection of bit errors separated by more than 10 bits.

Gap 3

The field begins following the last byte of the data EDAC bytes and is made up of one byte (for 256-byte sector) or 151 bytes (for a 2304-byte sector) extending to the next sector mark. This gap includes a one-byte end-of-field pad.

Gap 4

The field begins following the last sector on the track and continues to the Index Mark. It consists of 48 bytes of zeros.

ERROR RECOVERY TECHNIQUE

The MSC supports, internally, a number of automatically invoked recovery procedures that are described in the following paragraphs.

EDAC FUNCTIONALITY

The seven-byte EDAC field appended to the data field provides for the correction of error bursts of up to 11 bits and detection of bit errors separated by more than 10 bits.

During update read and write operations, the detection of any read error in an ID field will cause bit 4 of the Status Word to be set. The search (update read or write) will continue. If a successful search is not made prior to detection of two Index Marks, the operation is terminated with bit 4 set. Two retries are attempted before the operation is finally terminated. If a successful search is made prior to detection of two Index Marks, bit 4 is reset and the operation continues in a normal fashion. In neither case will any error correction be performed on the ID field.

If a read error is detected following the transfer of a sector data field to main memory, one of two situations is possible:

1. If the error is not correctable, a retry will be initiated (see Read Error Retry).
2. If the error is correctable, the MSC will automatically perform the required correction in main memory, set bit 9 of Status Word 1, and bit 0 of Status Word 2, and continue the data transfer operation. Note that the loss of a revolution of the media will occur during the correction period.

READ ERROR RETRY

If an uncorrectable read error is detected following transfer of a sector data field to main memory, the following retry procedure will be invoked automatically by the MSC:

1. Three retries
2. Three retries with clock retarded
3. Three retries with clock advanced
4. Three retries with offset in
5. Three retries with offset in, clock retarded
6. Three retries with offset in, clock advanced
7. Three retries with offset out
8. Three retries with offset out, clock retarded
9. Three retries with offset out, clock advanced

Note that:

- EDAC is attempted at each retry position.
- The read error retry is applied only to uncorrectable data field errors during Read Data commands (does not apply to format or diagnostic commands; bit 4 of Status Word 1 is set in these cases as applicable).
- A latency period is entered between retries, i.e., other channels on the MSC will be serviced if there is any activity on them.
- A loss of at least one revolution will occur for each retry.
- Any offset or clock change condition will be automatically restored after retry (successful or unsuccessful). These conditions will not be reset if caused as a result of any Tag Code In/Out command.

The read error retry has one of two results:

- If the error is not recoverable, bit 4 of Status Word 1 is set and the operation is terminated.
- If the error is recoverable, bit 9 of Status Word 1 and bit 1 of Status Word 2 are set and the data transfer operation is continued.

OVERRUN/UNDERRUN RETRY

If an underrun or overrun condition occurs during a Read or Write Data command, the data field affected will be retransmitted automatically by the MSC until the transfer is successful.

Note that:

- A latency period is entered between retries, i.e., other channels on the MSC will be serviced if there is any activity on them.
- A loss of at least one revolution will occur for each retry.

- The occurrence of an Overrun/Underrun retry will result in the setting of bit 9 in Status Word 1 and bit 2 in Status Word 2.
- Format and diagnostic commands will not be retried if an underrun/overrun condition occurs. This will result in the setting of bit 2 in Status Word 1.

INSTRUCTIONS

Table 2-1 lists the I/O commands to which the MSC9102 and disk units respond. A detailed description of each instruction follows this table.

TABLE 2-1. I/O BUS COMMANDS

Type	Function Code (Hex)	Description
Output	09[a]	Output Address
	0D	Output Range
	0F	Output Offset Range
	11	Output Configuration Word A
	13	Output Configuration Word B
	03	Output Interrupt Control
	07	Output Task Word
	01	Output Control Word
Input	08	Input Memory Byte Address
	0A	Input Memory Module Address
	0C	Input Range
	0E	Input Offset Range
	10	Input Configuration Word A
	12	Input Configuration Word B
	02	Input Interrupt Control
	26	Input Identification Code
	06	Input Task Word
	18	Input Status Word 1
	1A	Input Status Word 2

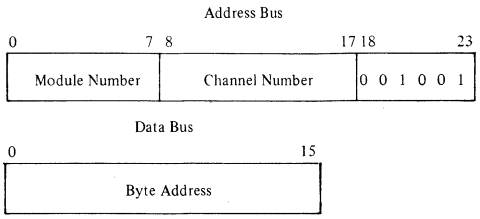
[a]Function Code 09 as executed by the CP results in execution of functions 09 and 0D.

OUTPUT COMMANDS

Command Output Address

Function Code 09

Format



Function

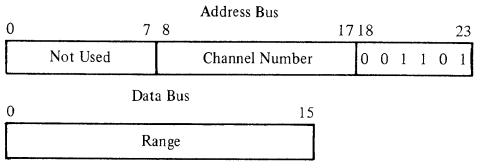
This instruction loads a 24-bit address into the address register associated with the referenced channel (unit). The address refers to the starting (byte) location in main memory where the MSC will start input or output data transfers. Bits 0-7 of the Address Bus (Module Number) are the most significant bits of the address. The data bus contains the 16 least significant bits. Data transfers to or from memory will normally be on a word basis, but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary.

Bit 17 of the Address Bus (direction bit of the channel number) determines the direction of any subsequent data transfer operation. A logical one specifies an output operation (writing on media), while a logical zero specifies an input operation (reading from media).

Command Output Range

Function Code 0D

Format



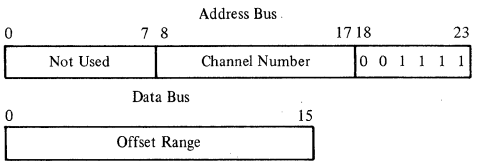
Function

This instruction loads the range register associated with the referenced channel. The (16-bit) quantity loaded (data bus) is the number of bytes to be transferred during the data transfer that is being set up. The number is a positive binary quantity (bit 0 must be zero) and is decremented by the MSC after each memory transfer. A range of zero will result in a premature end-of-operation termination for any Read (unless a nonzero offset range is specified) or Write command that may be subsequently issued (refer to Output Task Word command). Any range register residue will be applied to the next command unless reset by another IOLD instruction.

Command Output Offset Range

Function Code 0F

Format



Function

This instruction loads the output offset range register associated with the referenced channel. The (16-bit) quantity loaded (data bus) is the number of

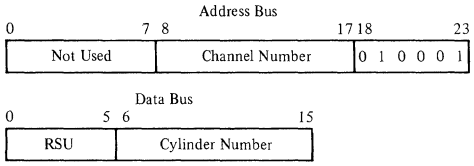
bytes to be discarded from the beginning of the data transfer prior to the transfer of any data to main memory. The output range is decremented only after the offset range register is decremented to zero.

The output offset range is used only in conjunction with Read operations (offset range ignored for Write operations) and must be set for each data transfer using an offset. The offset is a positive binary quantity and is decremented by the MSC after each byte read from the disk. Any offset range register residue will be applied to the next command unless reset by another output offset range instruction. Note that read errors encountered during any offset operation will terminate that operation as specified for any normal Read operation (refer to Output Task Word command). The offset range residue can be nonzero only as the result of an error. The offset range register can be used for media verification by setting the range register to zero and the offset range register for the number of bytes to be verified.

Command Output Configuration Word A

Function Code 11

Format



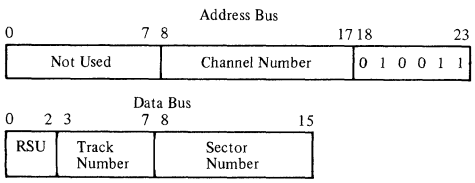
Function

This instruction loads Configuration Word A for the unit corresponding to the referenced channel. The cylinder address (bits 6-15) is used as the seek argument during Seek operations. The complete word is used as the two high-order bytes of a sector ID field to be searched for during a search and Read or Write operation. Bits 0-5 are reserved for software use (RSU). The maximum cylinder address permissible is 410 or 822.

Command Output Configuration Word B

Function Code 13

Format



Function

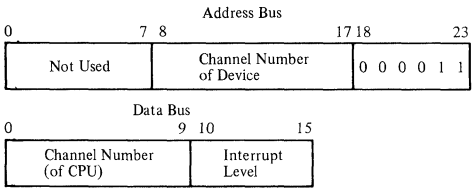
This instruction loads Configuration Word B for the unit corresponding to the referenced channel. This word is used as the two low-order bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 3-7 provide the track address for any Read or Write operations.

The subsystem will treat bits 8 through 15 of Configuration Word B as a sector number. This number will be incremented after operating on a data field during a data field Read or Write operation (refer to Output Task Word command). Note that if the automatic rotational position sensing function is used that the sector number must represent the physical sector on the track and that bits 8 and 9 must be zero. Bits 0 through 2 are reserved for software use (RSU).

Command Output Interrupt Control

Function Code 03

Format



Function

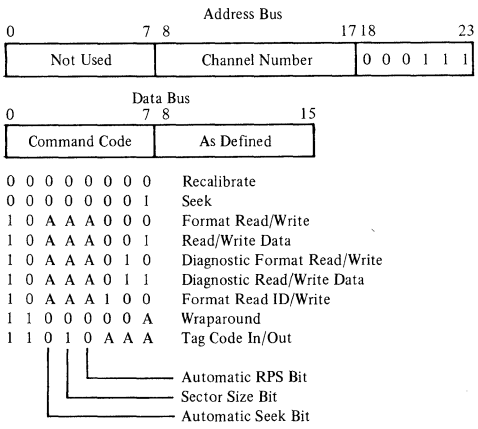
This instruction loads, for the referenced device, the interrupt level and the channel number of the CPU to which subsequent interrupts should be sent. The level number is a 6-bit quantity and is positioned on the data bus as shown. Bits 0-9 of the data bus contain the channel number to which subsequent interrupts are to be directed.

If an interrupt level of zero is loaded, the subsystem will not generate or save interrupts for any events that occur while the interrupt level is zero. The interrupt level is set to zero whenever the subsystem is initialized.

Command Output Task Word

Function Code 07

Format



Function

This instruction outputs a Task Word to the referenced channel. The coding of bits 0 through 7 represent the operations that are to be performed. When this instruction is accepted, the channel enters the busy state and the indicated task is initiated or stacked. All address, range, and configuration information must be loaded prior to execution of this instruction. The direction of data transfer is indicated in the low-order bit of the most recent output address instruction. For example, if the data field encoding of the Task Word is received when a "Read" channel number is indicated, then a Read Data command will be executed. Note that track selection is performed for each media data transfer command prior to the initiation of the data transfer and is based on the current contents of Configuration Word B.

Bits 2-4 of the command code have specific meaning for all media data transfers as follows:

1. Bit 2 — Automatic Seek
   If this bit is a logical zero, the data transfer will be initiated based on the current cylinder position of the unit.
   If this bit is a logical one, a Seek Cylinder operation, based on the current contents of Configuration Word A, will be initiated to the unit. Other channels may be serviced by the MSC during the seek latency period. At seek completion, no seek complete interrupt will be generated to the bus channel, and the specified data transfer operation will be initiated.
2. Bit 3 — Sector Size
   If this bit is a logical zero, data transfer operations will assume that the track selected is formatted with 256-byte sectors.
   If this bit is a logical one, data transfer operation will assume that the track selected is formatted with 2304-byte sectors.
3. Bit 4 — Automatic Rotational Position Sensing (RPS)
   If this bit is a logical zero, initiation of the data transfer operation will cause a search on the media for the ID specified in Configuration Word A and B (or the Index Mark in the case of format operations). This activity, will prevent initiation of a task on any other channel for the duration of the search and any subsquent data transfer. If this bit is a logical one, initiation of the data transfer operation will be preceded by an RPS command to the device based on the current sector number (bits 10-15 only) of Configuration Word B (bits 8 and 9 are ignored).The drive will notify the MSC when the requested sector number is on position. The MSC is free to execute any activity on any other channel (including a data transfer) after initiation of the RPS command to the unit. The indicated data transfer will be initiated when the ID field, indicated by Configuration Words A and B (or the Index Mark in the case of format operations), is found following the RPS on indication from the drive. Note that use of this facility requires that sectors be numbered sequentially on a track beginning with sector 0 and ending with sector 7 (for 2304 byte sectors) or 63 (for 256-byte sectors).

Bits 2 through 4 can be set in any combination (they present no interrelationships) for a data transfer operation.

In addition to the mentioned functionality, multisector data transfer operations (Read or Write), enable an automatic track and cylinder function. Track switching will occur whenever the last logical sector (sector 63 for 256-byte sectors or sector 7 for 2304-byte sectors) on the track has been completed and the range has not expired. Note that track switching is not associated with the Index Mark, but with the last sector number, i.e., only if the sector number is equal to 7 or 63, will track switching occur. When the last track of the cylinder has been completed and track switching is attempted, the MSC will initiate a seek to the next consecutive cylinder number, select track number zero, and initiate a search for sector number zero. Note that activities on other channels (including data transfers) may occur during the seek latency period.

Additional considerations are:

1. Data transfer continues until the range expires, an error is encountered, an unsuccessful search occurs, or the end of the last cylinder is detected (setting bit 5 of the Status Word).
2. Automatic track switching does not occur for any format operation or any unsuccessful search (detection of two Index Marks without a successful compare.
3. When track completion is detected without error, the Configuration Words will be modified to reflect the next consecutive track and sector zero. In addition, if cylinder completion is also detected, the Configuration Words will be modified to reflect the next consecutive cylinder, and track and sector zero. Note that this update will occur only if the range is not zero at the end of the last sector of the previous track.
4. An attempt to automatically switch off the last track of th last cylinder will result in status bit 5 being set.

An additional function of the task Word is that it will cause unit detailed status to be reset (via issuance of Tag Code 010 to the unit) unless the Task Word command is the Tag Code In/Out command, in which case unit detailed status will not be reset.

The command code can designate the following types of commands:

RECALIBRATE

The Recalibrate command causes the channel to move the unit's positioner to cylinder zero, select track zero, and reset the "Seek Timeout" line on the device interface. This instruction is intended as an Initialization command to guarantee that the positioner location information in the controller is correct and that all device faults are cleared. Completion of the recalibration operation by the unit will result in the generation of an appropriate interrupt.

SEEK

The Seek command in the Task Word causes the channel to move the unit's positioner to the cylinder indicated in Configuration Word A. If the cylinder specified is greater than 410 or 822 or an error occurs during positioner movement, then an error bit will be set in the Status Word. Completion of a positioning operation (whether or not any physical movement occurred) by the unit will result in the generation of an interrupt. Note that seek completion as a result of an automatic seek will not result in an interrupt.

FORMAT READ

The Format Read command causes the channel to read all identifier (ID) and data fields on a track beginning with the first sector after index and in the order in which they are recorded. Data will be transferred to memory beginning at the memory location specified in the subsystems memory address register (after any offset has been exhausted). This address will be the address loaded by the most recent output address IOLD instruction if no data transfer has occurred since that instruction was executed. If one or more data transfer operations have been executed since the last output address IOLD instruction, then the starting memory address used for this operation will be the byte address immediately following the end of the most recent data transfer (Read or Write) executed for this unit.

If bit 8 of the command code is a one, then the EDC bytes of any sector identifier read will be ignored. If bit 8 of the command code is a zero, then the EDC bytes of any sector identifier read will be checked.

Data will be transferred until an uncorrectable read error occurs (except as noted for bit 8), the range is satisfied, or the entire track is read (index is detected).

Normal range for this command (to read one complete track) is:

$R = (4 + 256) \times 64 = 16640$ bytes (for 256-byte sectors)

or

$R = (4 + 2304) \times 8 = 18464$ bytes (for 2304-byte sectors)

where:

4 = number of bytes in ID
256/2304 = data
64/8 = number of sectors per track

If this command is terminated due to end-of-track before the range is satisfied, the residual range will be available via the Input Range command. An uncorrectable read error in any field (except as previously noted for bit 8 of the command code = 1) will cause the operation to be terminated with the read error bit set in the Status Word (bit 4). The sector ID field in Configuration Word B will point to the sector in error if Configuration Word B was properly loaded and the sectors are numbered consecutively. The field in error can be determined through examination of the residual range (if a read error is detected in an ID field the range will have been decremented for the ID field only).

If the required transfer rate is not maintained on the megabus (600 KW/S), the operation will be terminated and the overrun/underrun bit will be set in the Status Word (bit 2).

If the range and offset range registers are zero when this command is received, the task will be immediately terminated (end-of-operation). No data will be read or transferred. Track selection for the operation is based on the current contents of the track address of Configuration Word B.

FORMAT READ ID

The Format Read ID command is identical to the Format Read command except that only the IDs of each sector are transferred to memory.

Normal range for this command (to read one complete track) is

$R = 4 \times 64 = 256$ bytes (for 256-byte sectors)

or

$R = 4 \times 8 = 32$ bytes (for 2304-byte sectors)

where:

4 = number of bytes in ID
64/8 = number of sectors per track

FORMAT WRITE

The Format Write command causes the channel to format the track which is positioned under the Read/Write head specified by Configuration Word B when this command is received. Eight or 64 (as specified by bit 3 of the Task Word) equal length sector will be written starting at index. The sector ID fields will be read from memory beginning with the memory location specified in the subsystem's memory address register.

Data fields will be written with data field sync words and will be zero filled by the MSC.

The range to format one complete track is:

$R = 4 \times 64 = 256$ bytes (for 256-byte sectors)

or

$R = 4 \times 8 = 32$ bytes (for 2304-byte sectors)

If a range other than that specified is sent for a Format Write, the remaining portion of the track will be zero filled. If the range was not a multiple of 4 bytes, the format of the last sector will be unspecified.

If the range register is zero when this command is received, the task will be immediately terminated (end-of-operation). No data will be written.

If the sector ID data cannot be read from memory at a sufficient rate, then the operation will be terminated and the overrun/underrun bit will be set in the Status Word (bit 2).

READ DATA

The Read Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to begin transfer of the data field of (at least) that sector to main memory. Data will be transferred to memory beginning with the memory location specified in the subsystem's memory address register after any offset has been exhausted and will continue until the range is satisfied.

When the transfer of the first specified sector data field is completed (without error), the sector number field of Configuration Word B will be incremented. If the initial range (range plus offset range) was greater than 256 (or 2304 if 2304-byte sectors are specified), then the sector on that track represented by the updated contents of Configuration Words A and B will be located and data transfer will continue with the new sector's data field. This operation will continue until the range is satisfied, an uncorrectable read error occurs, or the record specified by Configuration Words A and B cannot be located on the track (as indicated by the detection of two Index Marks without a successful compare). If the specified record cannot be located, an unsuccessful search will be posted in the Status Word (bit 7). Note that track and cylinder switching may occur.

Track selection for the operation is based on the current contents of the track address of Configuration Word B.

If an uncorrectable read error is encountered in a data field, the operation will be terminated and the read error bit in the Status Word will be set (bit 4). The sector number field of Configuration Word B will contain the address of the record in error. If a read error is encountered in an ID field, a mis-compare result will be assumed and the search will continue. In this case, the read error bit will be posted in the Status Word so that if the desired record is never located, the operation will be terminated with both the unsuccessful search bit and read error bit posted in the Status Word indicating that the reason for the mis-compare could be a read error in the sector ID. If the search is eventually successful, the read error bit in the Status Word will be reset.

If this command is terminated before the range is satisfied, the residual range will be available via the Input Range command. If the range and offset range registers are zero when this command is received, the task will be immediately terminated (end-of-operation). No data will be read or transferred.

If the required transfer rate is not maintained on the megabus (600 KW/S), then the operation will be terminated and the overrun/underrun bit will be set in the Status Word (bit 2).

WRITE DATA

The Write Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to rewrite the data field of at least that sector. The data will be read from memory beginning with the memory location specified in the subsystem's memory address register. Rewritten data fields will be preceded by data field sync words. When the transfer of the specified sector is completed, the sector number field of Configuration Word B will be incremented.

If the range is less than 256 or 2304, the remainder of the data field will be zero filled. If the range was greater than 256 or 2304, the sector represented by the updated contents of Configuration Words A and B will be located and the data field rewritten (preceded by a data field sync word). This operation will continue until either the range is satisfied or the record specified by Configuration Words A and B cannot be located on the track (as indicated by the detection of two Index Marks without a successful ID field compare). If the latter event occurs, unsuccessful search will be posted in the Status Word (bit 7). Note that track and cylinder switching may occur.

If a read error is encountered in an ID field, the ID value will be ignored and the search will continue. In this case, the read error bit will be posted in the Status Word so that if the desired record is not located, the operation will be terminated with both the unsuccessful search bit and the read error bit posted in the Status Word indicating that the reason for the mis-compare could be a read error in the sector ID. If the search is eventually successful, the read error bit in the Status Word will be reset.

If this command is terminated before the range is satisfied, the residual range will be available via the Input Range command. If the rag register is zero when this command is received, the task will be immediately terminated (end-of-operation). No data will be written.

If the required transfer rate is not maintained on the megabus (600 KW/S), the operation will be terminated and the overrun/underrun bit will be set in the Status Word (bit 2).

Track selection for the operation is based on the current contents of the track address of Configuration Word B.

DIAGNOSTIC WRITE DATA

The Diagnostic Write Data command causes the channel to perform as if the Write Data command

were specified except that EDAC characters will be written at the end of the data field updated as read from memory (not hardware generated). Only one sector can be updated by this command so that the range must equal 263 or 2311 bytes.

Track selection for the operation is based on the current contents of the track address of Configuration Word B.

DIAGNOSTIC READ DATA

The Diagnostic Read Data command causes the channel to perform as if the Read Data command were specified except that the seven-byte EDAC field attached to the data field will also be transferred to memory (error detection/correction of the data field is not performed). Only one sector can be read by this command so that the range must equal 263 or 2311 bytes.

Track selection for the operation is based on the current contents of the track address of Configuration Word B.

DIAGNOSTIC FORMAT WRITE

The Diagnostic Format Write command causes the channel to perform as if the Format Write command were specified except that invalid EDC characters will be written at the end of each ID field (the EDC characters will always be zero). Note that the data written in the data fields will be all zeros.

DIAGNOSTIC FORMAT READ

The Diagnostic Format Read command causes the channel to read everything on a track (including gaps, sync words, ID and data fields, EDC, and EDAC bytes) beginning with the first ID after the next Address Mark detected. Meaningful operation of this command can only be guaranteed on tracks which have not been updated since the last format operation (updated records may contain write splice discontinuities). No EDAC or EDC checks will be done. Data will be transferred until the range is satisfied.

If this command is terminated due to the second index pulse before the range is satisfied, the residual range will be available via the Input Range command.

If the required transfer rate is not maintained on the megabus (600 KW/S), the operation will be terminated and the overrun/underrun bit will be set in the Status Word (bit 2). Track selection for the operation is based on the current contents of the track address of Configuration Word B.

WRAPAROUND READ/WRITE

Two wraparound levels are available in the MSC/device adapter and are controlled by bit 7 (of the Task Word). If bit 7 is a logical one, the wraparound level is at the MSC level. In either case, functionality is as described in the following paragraphs.

During a Wraparound Write command, the channel will read 1 to 8 words from memory (at the address specified in the subsystem's memory address register and transfer the bytes to the appropriate (MSC or device adapter) first-in/first-out (FIFO) buffer.

When a Wraparound Read command is received (immediately following a Wraparound Write) the bytes previously loaded into the specified FIFO buffer by the previous Wraparound Write command, will be returned to main memory at the address specified in the subsystem's memory add register. The bytes returned during this operation will be the same as the bytes supplied by software in the preceding Wraparound Write command. The range specified for the Wraparound Write must be the same as the range specified for the Wraparound Read or the results are unspecified.

A range of 1 to 8 words should be specified for these commands. If range and offset range of zero is specified, the command will be immediately terminated (without being executed nor with any status indications). If a range greater than 8 words is specified, the results will be unspecified, except if bit 7 was a logical one, the overrun bit (bit 2) of the Status Word will be set and the command will be terminated immediately. In any case, the Wraparound Write and its associated Wraparound Read must start and end from the same memory boundary (byte or word).

Execution of a task instruction to any other channel during wraparound sequence will result in unspecified results.

TAG CODE IN/OUT

The Tag Code In/Out command provides an input/output capability for tag codes. The direction of transfer is determined by the direction bit of the last IOLD instruction for the channel. Bits 5, 6, and 7 of the command code determine which tag code is to be accessed (see Table 2-2).

When a tag code is output, the tag data placed on the device data bus is the data contained in bits 8-15 of the data bus. Only one tag code can be output to the unit per Task Word.

When a tag code is input, the tag code byte specified will be stored in the memory location indicated by the IOLD. The contents of bits 8-15 of the data bus will be placed on the device data bus, but not strobed. If the range specifies more than one byte, the tag code will be incremented so that consecutive tag code data bytes can be stored by this command. Multiple byte transfers will begin with the tag code specified and end with the expiration of the range or tag code 7.

TABLE 2-2. TAG CODE DECODING

BUS OUT

BITS / TAG CODE	0	1	2	3	4	5	6	7
Select 000	0	0	0	0	2^3	2^2	2^1	2^0
Error Recovery 001	EARLY STROBE	LATE STROBE	+ OFFSET	- OFFSET	0	0	0	0
Diagnostic 010	RECALI-BRATE	CLEAR ATTEN-TION	CLEAR CHECK DIAG.	CLEAR FAULT STATUS	CLEAR ERROR RECOVERY	CLEAR RPS	0	0
Head Address 011	0	0	0	2^4	2^3	2^2	2^1	2^0
High Cyl 100	0	0	0	0	0	0	2^9	2^8
Target Register 101	LOAD TARGET REGISTER	0	2^5	2^4	2^3	2^2	2^1	2^0
Low Cyl 110	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Control 111	TRANSFER SECTOR COUNT	WRITE GATE	0	READ GATE	ADDRESS MARK ENABLE	0	0	0

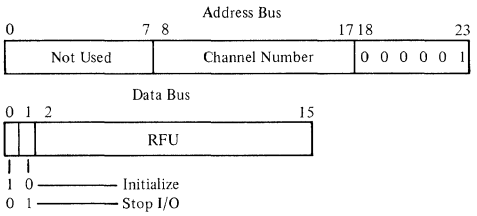
BUS IN

0	1	2	3	4	5	6	7
822 CYL	0	R F U	ATTEN-TION	2^3	2^2	2^1	2^0
BUS OUT BIT 0	BUS OUT BIT 1	BUS OUT BIT 2	BUS OUT BIT 3	BUS OUT BIT 4	BUS OUT BIT 5	BUS OUT BIT 6	BUS OUT BIT 7
NO HEAD SELECT	WRITE FAULT	(W/R) OFF CYL.	W+R FAULT	VOLT. FAULT	HEAD SELECT FAULT	SEEK ERROR	WRITE PROTECTED
START	SPEED	LOAD + RETURN TO 0	DIBIT FAULT	HEADS LOADED	SLOPE	FINE	0
ECHO READ TARGET REGISTER	0	2^5	2^4	2^3	2^2	2^1	2^0
ECHO READ TARGET REGISTER	0	2^5	2^4	2^3	2^2	2^1	2^0
ADDRESS MARK FOUND	0	ON CYL	UNIT READY	0	0	OFFSET ACTIVE	CHECK DIAG.
ADDRESS MARK FOUND	0	ON CYL	UNIT READY	0	0	OFFSET ACTIVE	CHECK DIAG.

Command Output Control Word

Function Code 01

Format



Function

This instruction loads a control word into the referenced channel. This command will be unconditionally accepted by the channel regardless of its busy status.

INITIALIZE

This command will cause the MSC to reset to the same state that it enters after power up. When an initialize command is received by the MSC, all of its channels are initialized (regardless of which channel the command was received over) A recalibrate will be executed on all disk units.

Operations that are in progress in the MSC at the time of the initialization will be abruptly terminated and all software addressable registers will be initialized. No information about the terminated operations will be retained and no interrupts for the operations will be generated. The interrupt level for all channels will be set to zero (interrupts blocked). Note that execution of this command may result in invalid data on the media (if a Write command was in progress) or a device fault (if a Seek was in progress at the drive).

STOP I/O

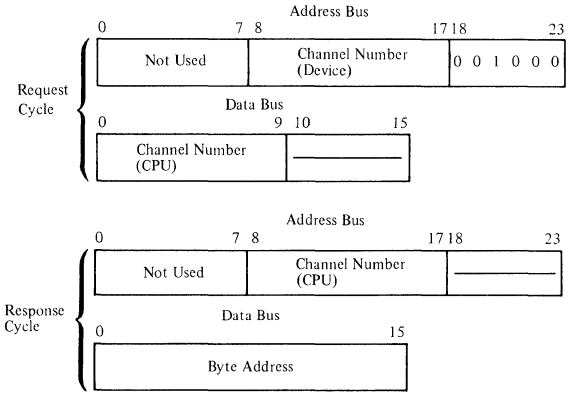
This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress, it will not be completed nor will any error checking be done. An interrupt will be generated for the operation terminated by this command as if the operation had come to a normal ending point. Status, address, and range information, present in the MSC when this command is received, will be retained. Note that execution of this command may result in invalid data on the media (if a Write operation was in progress) or a device fault (if a Seek operation had been initiated and not completed prior to a subsequent operation).

INPUT COMMANDS

Command Input Memory Byte Address

Function Code 08

Format



Function

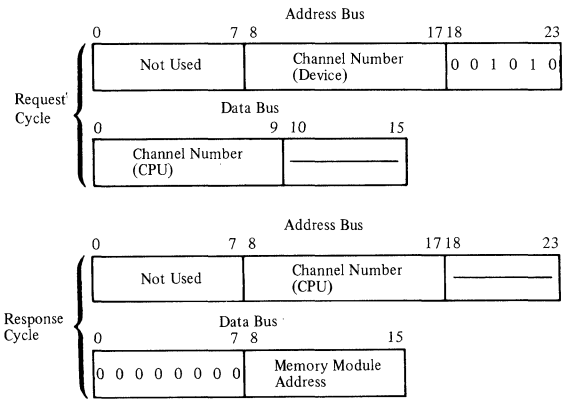
This instruction causes the current contents of the referenced channel's memory byte address to be transferred to the requesting channel.

During the response cycle (Second Half Read), the MSC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle. The data bus will contain the 16 low-order bits of the memory byte address currently stored for the specified channel in the MSC. Note that if a Write command ended at a byte boundary (6 high-order bits of word), the memory address will reflect the next word (not the 8 low-order bits of the previous word). This command is used for diagnostic purposes only.

Command Input Memory Module Address

Function Code 0A

Format



Function

This instruction causes the current contents of the referenced channel's memory module address to be transferred to the requesting channel.

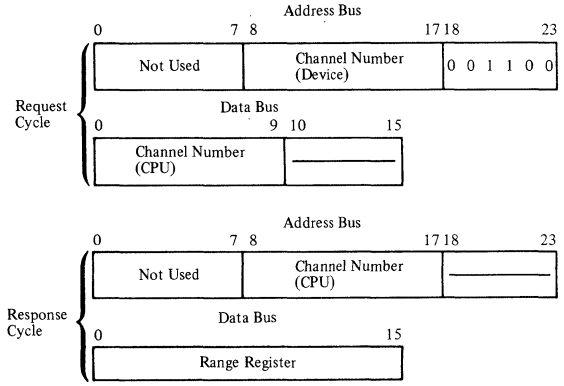
During the response cycle (Second Half Read), the MSC will return in bits 8-23 of the address bus the same data that was received in bits 0-15 of the data bus during the request cycle. The data bus will contain the 8 high-order bits of the memory word

address currently stored for the specified channel in the MSC. This command is used for diagnostic purposes only.

Command Input Range

Function Code 0C

Format



Function

This instruction causes the current contents of the referenced channel's range register to be transferred to the requesting channel.

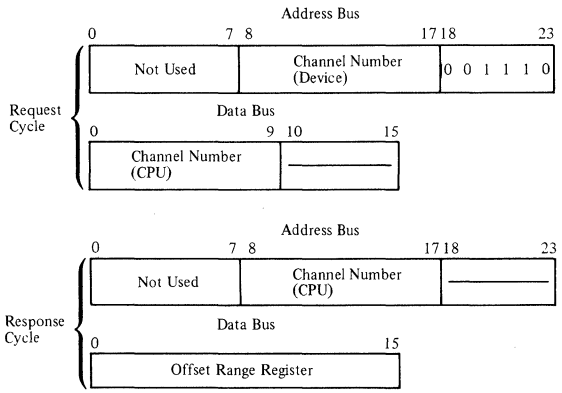
During the response cycle (Second Half Read), the MSC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

After the completion of a data transfer operation, the contents of the range register reflect the status of the transfer with respect to the physical sector(s) read.

Command Input Offset Range

Function Code 0E

Format



Function

This instruction causes the current contents of the referenced channel's offset range register to be transferred to the requesting channel.

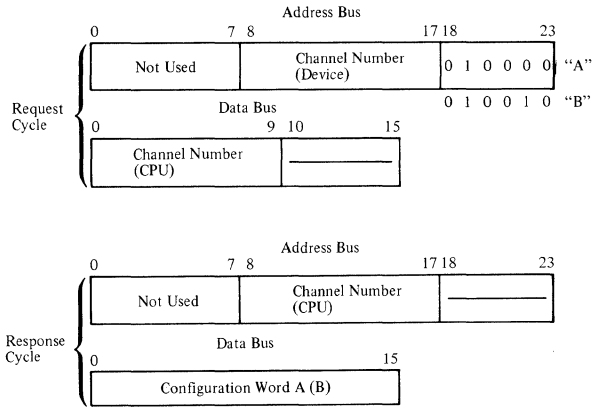
During the response cycle (Second Half Read), the MSC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

After completion of a data transfer operation, the contents of the offset range register reflect the status of that transfer with respect to the physical sector(s) read.

Command Input Configuration Word A (B)

Function Code 10 (12)

Format



Function

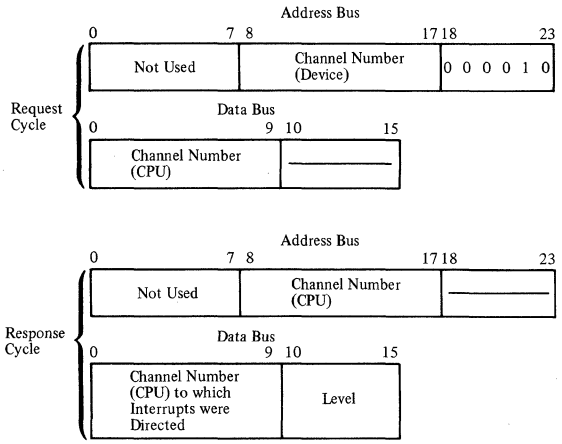
This instruction causes the current contents of the channel's Configuration Word A (B) to be transferred to the requesting channel.

During the response cycle (Second Half Read), the MSC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command Input Interrupt Control

Function Code 02

Format



Function

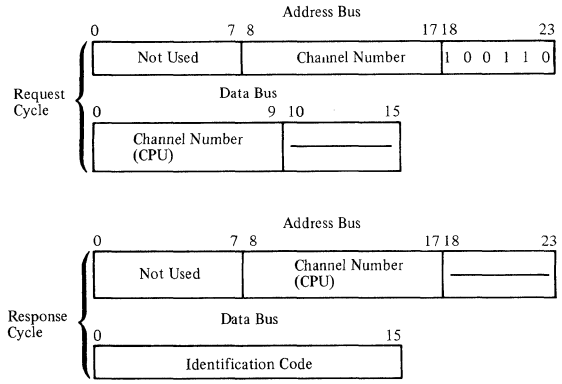
This instruction causes the channel's interrupt level to be transferred to the requesting channel. The level value will be placed on data bus bits 10 through 15 with bit 15 as the least significant bit. This quantity is the value previously received in an Output Interrupt Control instruction, or, a default value of 00. The default value is the interrupt level assumed by the channel when initialized. Note that the channel number returned in bits 0-9 of the data bus might be different than the channel number of the CPU executing this instruction if more than one CPU is attached to the megabus.

During the response cycle (Second Half Read), the MSC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command Input Identification Code

Function Code 26

Format



Function

This instruction will cause the referenced channel to transfer its identification code to the requesting channel. Depending on the unit accessed, one of the following codes will be returned.

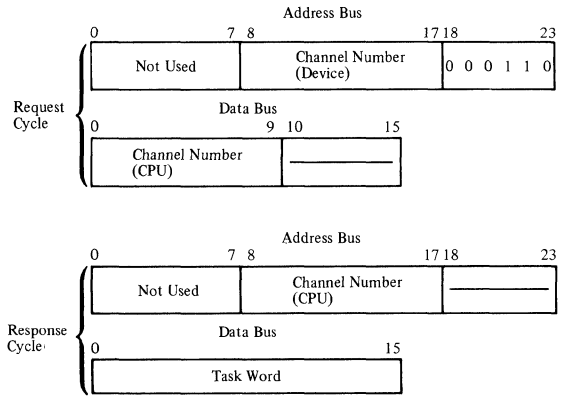
Code (Hex)	Model
2360	MSU9101/9105 (37MB)
2361	MSU9102/9106 (75MB)
2362	MSU9103 (144MB)
2363	MSU9104 (288MB)
236F	This code represents the ID code received when a unit is physically attached, but is not accessible to the system because it was not powered up. The ID will be reported as 236F. The MSC will generate the correct ID when the unit becomes available (i.e., when it is cycled up). This updated ID code is visible to software as the result of the execution of another Input Identification Code instruction.

During the response cycle (Second Half Read) the MSC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command Input Task Word

Function Code 06

Format



Function

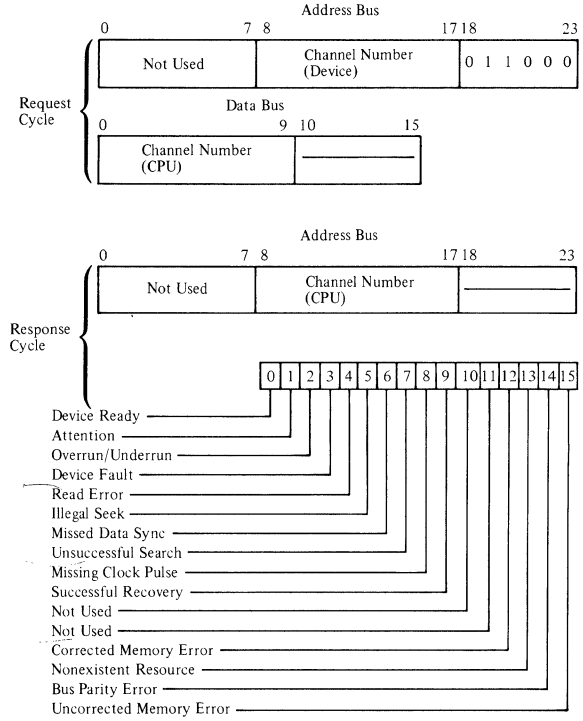
This instruction causes the Task Word of the referenced channel to be transferred to the requesting channel. The Task Word transferred will contain the code for the last operation executed by the channel (unless an Initialize has occurred).

During the response cycle (Second Half Read) the MSC will return in bits 8-23 the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command: Input Status Word 1

Function Code: 18

Format



Function

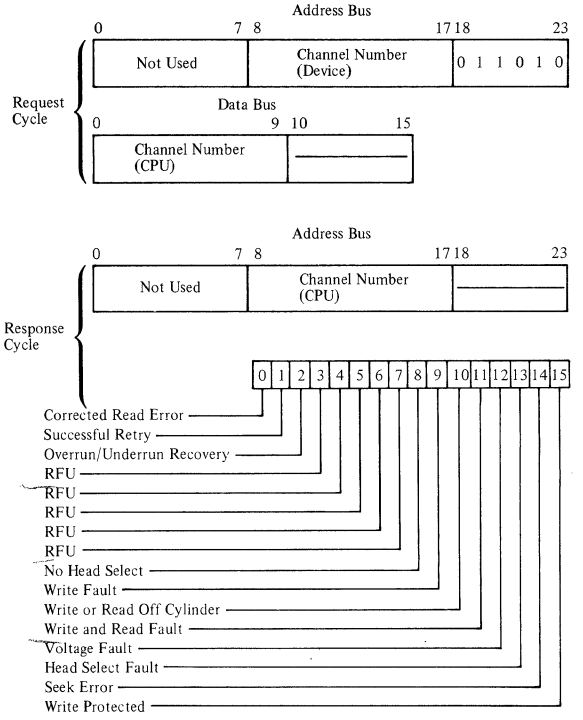
This instruction causes the referenced channel's Status Word 1 to be transferred to the requesting channel.

During the response cycle (Second Half Read) the MSC returns in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle. See Table 2-3.

Command: Input Status Word 2

Function Code: 1A

Format



Function

This instruction causes the referenced channel's Status Word 2 to be transferred to the requesting channel.

During the response cycle (Second Half Read) the MSC returns in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle. See Table 2-4.

TABLE 2-3. STATUS BIT DEFINITIONS — INPUT STATUS WORD 1

Status Condition	Bit	Definition	Reset By
Device Ready	0	The unit is online with the medium loaded and no further manual intervention is required to place it under program control. Note that a change of state of this bit will cause the attention bit (bit 1) to be set resulting in an interrupt (if the interrupt level is nonzero).	A change in condition
Attention	1	Set whenever the device ready bit (bit 0 of the Status Word) changed state. Indicates to software any change of operational status of the device (e.g., load/unload of media). Whenever set, an interrupt is attempted (if the interrupt level is nonzero). If a previously initiated operation is in progress when a device state change is sensed, the resultant interrupt (with the attention bit set) serves as notification of both the end of the operation and the device state change.	Input Status Word or Output Task Word[a]

TABLE 2-3 (CONT). STATUS BIT DEFINITIONS — INPUT STATUS WORD 1

Status Condition	Bit	Definition	Reset By
Overrun/Underrun	2	Set during a Read or Write operation when the data transfer to/from main memory cannot be maintained at a high enough rate (600K words per second during field transfers in word mode). Either data was lost on input due to a failure to keep up with unit demands or data was unavailable on output when required by the device.	Output Task Word[a]
Device Fault	3	Set if the check diagnostic bit (bit 7 of Tag Code 111 In) is set indicating a device fault. Bits 8-15 of Status Word 2 reflect the specific fault. Operator intervention is required to reset the Write Protect condition of the unit (assuming it is not due to a positioner offset).	Output Task Word[a]
Read Error	4	Set during any Read operation if the EDAC word at the end of a field indicates that an uncorrectable data error has occurred within the field. This bit will also be set in conjunction with an unsuccessful search/format error (bit 7) if a read error was detected in the ID field and the record could not be found.	Output Task Word[a]
Illegal Seek	5	Set if bits 6-15 of Configuration Word A exceed the maximum cylinder number for a device during a Seek command execution or a multisector operation.	Output Task Word[a]
Missed Data Sync	6	Set if, after a sector ID has been detected during any Read operation, the corresponding data field is not detected.	Output Task Word[a]
Unsuccessful Search/Format Error	7	Set during a nonformat Read or Write operation for which the sector ID specified in Configuration Words A and B cannot be located on the track. Also set if an Index Mark is detected during a Format Read/Write operation and in this case, memory address register is invalid.	Output Task Word[a]
Missing Clock Pulse	8	Set if the controller detects a missing clock pulse during Write operations. Note that a missing clock pulse during a Read operation results in a read error.	Output Task Word[a]
Successful Recovery	9	Set when a recoverable error condition was successfully recovered during the previous operation. Status Word 2 specifies the error condition which had occurred.	Output Task Word[a]
Not Used	10		
Not Used	11		
Corrected Memory Error	12	Indicates that during execution of the previous disk write operation main memory detected and corrected a memory read error. Data delivered to the MSC was assumed to be correct.	Output Task Word[a]
Nonexistent Resource	13	Set whenever the MSC attempts a bus cycle (except interrupt) and receives a NAK response from memory.	Output Task Word[a] or Input Status Word 1
Bus Parity Error	14	Set whenever the MSC detects a parity error on either byte of the data bus during any bus cycle, or when a parity error is detected in bits 0-7 of the address bus.	
Noncorrectable Memory Error	15	Indicates that during execution of the previous disk write operation, main memory detected a memory read error which the EDAC algorithm would not correct. Data delivered to the MSC was incorrect. It will not cause termination of the operation in progress (may result in bad data written on the medium).	Output Task Word[a]

[a]Initialize (output control word) and Master Clear on the bus also resets these status bits.

TABLE 2-4. STATUS BIT DEFINITIONS — INPUT STATUS WORD 2

Status Condition	Bit	Definition	Reset By
Corrected Read Error	0	Set when a correctable read error occurred during the previous read operation. Correction was performed by the MSC in main memory. When this bit is set, it also will cause bit 9 of Status Word 1 to be set.	Output Task Word[a]
Successful Retry	1	Set when a data read error has been successfully retried during the previous operation. Data stored in main memory is correct. When this bit is set, it will also cause bit 9 of Status Word 1 to be set.	Output Task Word[a]
Overrun/Underrun Recovery	2	Set when an underrun/overrun error has been successfully retried during the previous operation. Data stored in main memory or the media is correct. When this bit is set, it will cause bit 9 of Status Word 1 to be set.	Output Task Word[a]
Not Used	3-7		
		Note: Bits 8-15 are the device detailed status bits, which correspond to Tag Code 010, bits 0-7 respectively. If any of these bits are set, bit 3 of Status Word 1 will be set. These bits reflect the current status of the device. Note that the Write Protect indicator may not cause the device fault bit to be set.	
No Head Select	8	Set when a Head Select command greater than four has been selected. This will be cleared by selecting a valid head count.	Change in condition
Write Fault	9	Set when there is an absence of Write Current when the Write Gate is on. Detection of this fault inhibits the write in order to prevent destruction of data.	Change in condition
Write or Read and Off Cylinder	10	Set when a Write or Read operation has been attempted while the heads are not on cylinder. Detection of this fault inhibits writing.	Change in condition
Write and Read Fault	11	Set when the Write Gate is on at the same time as the Read Gate. Detection of this fault inhibits writing.	Change in condition
Voltage Fault	12	Set when a below normal voltage condition has been detected. Detection of a voltage fault inhibits writing and commands an emergency retract of the heads.	Change in condition
Head Select Fault	13	Set when more than one head has been selected. Detection of this fault inhibits writing.	Change in condition
Seek Error	14	Set when a seek error has occurred. This signal indicates that the unit was unable to complete a move within 500 ms, or that the carriage has moved to a position outside the recording field, or that an address greater than 822 cylinders has been selected. If an address greater than 822 cylinders is selected, the seek error signal will go true within 100 ns of the execution of load low cylinder (Tag 110). A seek error can only be cleared by performing a Recalibrate operation.	Change in condition
Write Protected	15	Set when the device is write protected. This signal may occur during fault conditions that inhibit writing or when write protection is desired on a unit by pressing its protect switch. If the Write Gate becomes true when the drive is write protected, then the check diagnostic bit will become true. The write protected condition can be cleared by pressing the units "protect" switch.	Change in condition

[a]Initialize (output control word) and Master Clear on the bus also resets these status bits.

Section 3
Controls and Indicators

This section describes the various controls and indicators necessary to the operation of the disk units.

OPERATOR CONTROL PANEL

The operator control panel for each disk unit contains four light-emitting diode (LED) indicators, three push buttons, and a unit select plug (see Figure 3-1). Table 3-1 lists and describes these controls and indicators.

POWER SUPPLY CONTROL PANEL

Table 3-2 lists and describes the various controls pertaining to disk unit power (see also Figure 3-2).

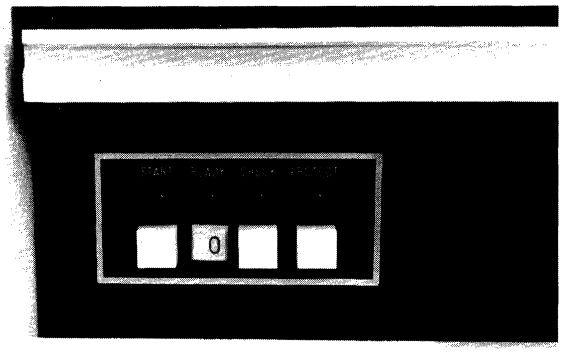
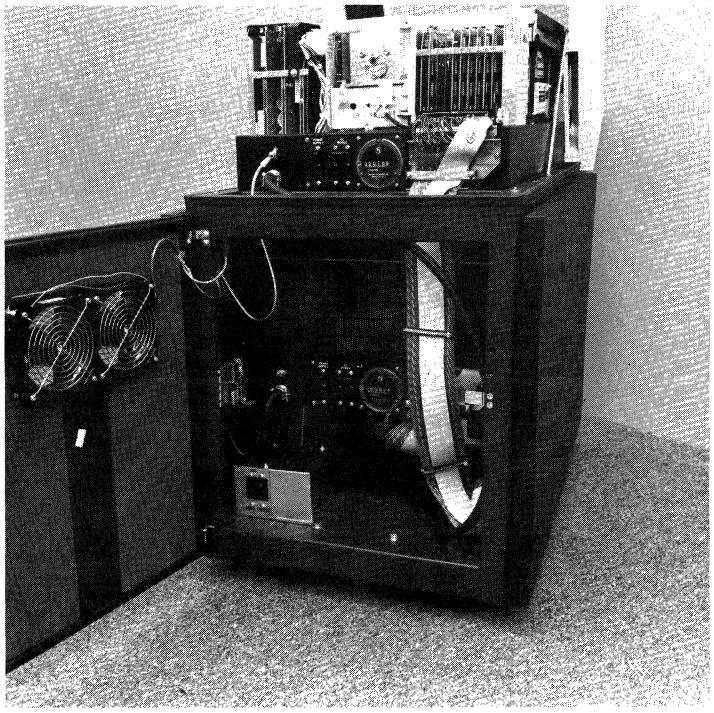


Figure 3-1. Operator Control Panel

TABLE 3-1. OPERATOR CONTROL PANEL CONTROLS AND INDICATORS

Control/Indicator	Description
START (Push Button/Indicator)	LED lights (red) when spindle is started. If controller is powered up, the unit may be started by pressing the START button (or it will start if the START button had been previously pushed). Press the button to start power on/off sequence as appropriate.
READY (Indicator)	LED lights (red) when the spindle is rotating at the proper speed, the heads are loaded, no fault condition exists, and the unit is ready to accept commands.
CHECK (Push Button/Indicator)	LED lights (red) when a fault condition exists. After correcting the problem, press the button to clear the condition and reset the indicator.
PROTECT (Push Button/Indicator)	LED lights (red) when the unit is in protect and writing on the disk pack is inhibited. Press the button to select the appropriate write/permit mode.
Unit Select Plug	When inserted, the unit select plug determines the logical identifier number (0-3) transmitted by command to the appropriate port in the MSC. When the plug is removed, the unit cannot be addressed. **Note:** The uncoded unit select plug supplied with each unit must be encoded by the Honeywell Field Engineer during installation. Once encoded, the number of the plug may not be changed. Additional uncoded plug kits are available as an accessory. Plugs may be interchanged among units.



MSU9101/9102/9105/9106

MSU9103/9104

Figure 3-2. Power Supply Control Panel

TABLE 3-2. POWER SUPPLY CONTROL PANEL CONTROLS

Control	Description
	MSU9101/9102/9105/9106
MAIN POWER (Circuit Breaker)	Controls primary power to disk unit(s). Located inside rear door of each cabinet on the floor.
AC POWER (Circuit Breaker)	Controls ac power to the blower and elapsed time meter of each unit. Located inside the rear door of each cabinet and for each unit.
POWER SUPPLY (Circuit Breaker)	Controls power to the power supply of each unit. Located inside the rear door of each cabinet and for each unit.
	MSU9103/9104
MAIN AC (Circuit Breaker)	Controls ac power to each unit. Located inside the rear door of each cabinet.
HOURS (Elapsed Time Meter)	Records accumulated ac power-on time. Meter starts when MAIN AC breaker is set to ON.
LOCAL/REMOTE (Switch)	In the REMOTE position, the unit cannot start (when START pressed) unless the controller is powered up. In the LOCAL position, an override enables the unit to be started when START is pressed. The normal position for the switch is in the REMOTE position. This switch is for use by Honeywell Field Engineering.
+20V, MOTOR, +46, −46, +9.7, −9.7, +20, −20, +28	Controls associated voltages to unit and overload protection.

Section 4
Operation

This section describes the operating and maintenance procedures.

POWER-UP PROCEDURE

In the following procedure, it is assumed that all cables have been properly connected and secured and that power is supplied to the unit.

1. Open rear door of cabinet (see Figure 3-2).
2. Set MAIN POWER/MAIN AC circuit breaker to ON.
   - Observe that blowers start.

   CAUTION

   Allow blowers to operate for at least two minutes before installing disk pack.

3. Close rear cabinet door.
4. Refer to Disk Pack Loading Procedures.
5. Press START button.

POWER-DOWN PROCEDURE

1. Press START button.
   - Heads unload, spindle stops, and LED indicators for START and READY extinguish.
2. Pull out drawer, if applicable.
3. Open cover and remove disk pack.
4. Close cover (and drawer).
5. Open rear cabinet door.
6. Set MAIN POWER/MAIN AC circuit breaker to OFF (see Figure 3-2).
7. Close rear cabinet door.

DISK PACK LOADING

Make certain that the disk pack to be mounted has been cleaned and maintained properly.

1. Verify that the START LED indicator is extinguished.

   CAUTION

   Never attempt to open the cover when the START LED indicator is lighted as this will cause the heads to unload and the spindle to stop.

2. Pull out the drawer, if applicable.
3. Press the latch and open the pack access cover.

   CAUTION

   Make certain that no dust or other foreign particles are present in shroud area. Also, ensure that blowers operate for at least two minutes prior to disk pack installation.

4. Disengage bottom dust cover from disk pack by squeezing the release lever mechanism in center of bottom dust cover and set cover aside to an uncontaminated storage area.

   CAUTION

   Make certain the heads are fully retracted before installing the disk pack.

5. Set disk pack on spindle, avoiding abusive contact between disk pack and spindle, then twist clockwise until it is secured to spindle lockshaft (see Figure 4-1).

   Note:

   Top dust cover actuates a brake when pack is set on spindle. Actuating brake holds spindle stationary while pack is installed. A click is heard as brake engages.

Figure 4-1. Disk Pack Loading

6. Lift top dust cover clear of unit and store it with bottom dust cover.

CAUTION

Spin pack to ensure that removing top dust cover released brake.

7. Close pack access cover immediately to prevent entry of dust and contamination of disk surfaces.
8. Close drawer, if applicable.
9. Refer to Start-up Procedure.

START-UP PROCEDURE

1. Make sure appropriate unit select plug is inserted.
2. Press START button.
   - START LED lights and after spindle gets up to speed, heads load and READY LED lights.
3. Press PROTECT button to select the appropriate write/permit mode.

   Note:

   PROTECT button LED lights if in protect mode.

DISK PACK UNLOADING

1. Press START button.
   - Heads unload, spindle stops and LED indicators START and READY extinguish.
2. Pull out drawer, if applicable.
3. Open pack access cover.

CAUTION

Make certain heads are fully retracted before removing disk pack.

4. Place top dust cover over disk pack so post protruding from center of disk pack is received into dust cover handle.
5. Turn cover counterclockwise until disk pack is free of spindle.

CAUTION

Avoid abusive contact between disk pack and spindle.

6. Lift top cover and disk pack clear of unit and close pack access cover (and drawer) unless another disk pack is to be loaded.
7. Place bottom dust cover on disk pack and store pack in an uncontaminated storage area.

DISK PACK HANDLING AND STORAGE

The following common sense rules are the prerequisites for proper disk pack handling:

- Always keep a disk pack in its carrying case whenever it is not on a disk pack drive.
- The bottom cover of the disk pack carrying case may be removed easily by squeezing the latch on the bottom cover; the top cover is designed so that it cannot be removed until the disk pack is mounted on the spindle.
- Always reassemble the disk pack carrying case covers even when the disk pack is not inside.
- Never touch disk pack recording surfaces or the spindle mating surface with anything.
- Do not expose a disk pack to stray magnetic fields, excessive pressure, sharp impact, or direct sunlight.
- Return every disk pack to its own carrying case.
- Never store a disk pack where the temperature exceeds 60° to 90°F (15°C to 32°C). If the limit has been accidentally exceeded, keep the disk pack in the operating room temperature for two hours before it is used.
- Store a disk pack in an environment identical to the disk pack drive operating environment.
- Store a disk pack flat, resting on its bottom cover. Never store a disk pack on edge.

GENERAL CLEANING

Operators should keep cabinets clear and free of dust. The disk pack chamber and spindle may be cleaned with a lint-free industrial cleaning tissue lightly dampened with an approved cleaning alcohol.

FILTER CLEANING

1. Remove filter which slides out from under the bottom of the cabinet (see Figure 4-2). The filter is accessed from the front on the MSU9101/9102/9105/9106 units and from the rear on the MSU9103/9104 units.
2. Tap filter over a bin to remove any loose dirt.
3. Vacuum filter.
4. Replace filter.

MSU9101/9102/9105/9106

MSU9103/9104

Figure 4-2. Filter Location

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